Vote Address Selection and Timely Initialization for High Frame Rate and Ultra-low Delay Hough Transform

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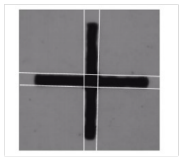
Research background

Straight Line

Prominent geometric feature of human made objects



Fast feature-based search and location

Indoor positioning of robots

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Straight-line detection

Help with swifter and continuous responses in factory automation

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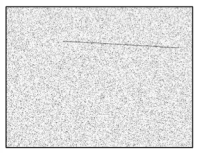
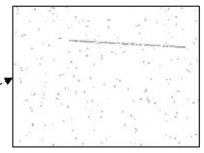
A front-end visual task that requires high frame rate and ultra -low delay

Proposed method



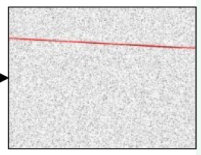
Edge detection



ρ_θ calculation

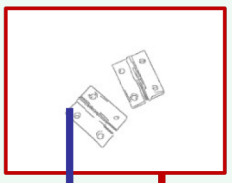
Hough space access (vote)

Search in the Hough space



Proposal 1: 4-to-1 vote address selection for Hough transform

Proposal 2: Timely switch between vote and initialization

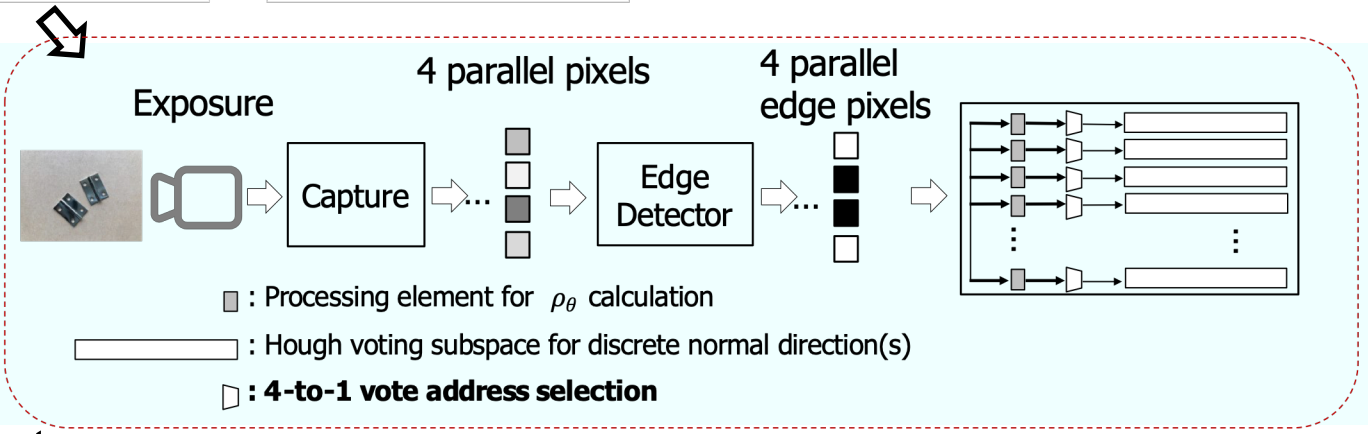


voted address

Hough voting space

Pixels on image border: set 0 to the addressed memory cell

Pixels in image (except border pixels): voting as usual

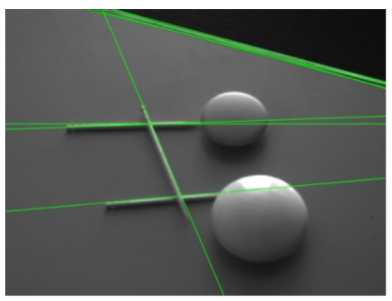


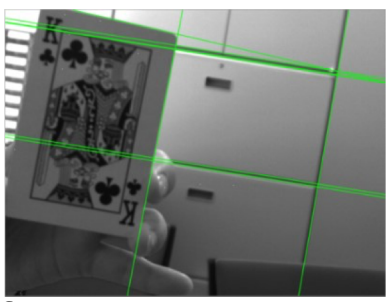
Experiments

Item	Straight-line detection core
# LUT	22561 (11.07%)
# LUTRAM	157 (0.25%)
# Flip Flop	28137 (6.90%)
# BRAM	94 (21.12%)
# IO	311 (62.20%)
# of cycle	693
Input frequency	100 MHz
Processing delay (640 × 480 frame)	0.7749 ms/frame

# of cycle: the number of clock cycles the detection core needs to finish processing the parallel 4 pixels.

FPGA: Xilinx Kintex-7 XC7K325T





Root mean square error for accuracy measure

Method Name	Error θ (rad)	Error ρ (pixel)
Standard HT	0.0057	2.13
Chern et al. ICPADS 2005	0.0057	2.08
Chen et al. VLSI 2011	0.0058	2.35
Northcote et al. ISCAS 2018	0.0119	2.01
Ours	0.0057	2.15

Conclusion

The evaluation result shows that the proposals achieve as accurate detection (Root Mean Square Error (RMSE) of θ on 0.0057, and RMSE of ρ on 2.15) as standard Hough transform (RMSE of θ on 0.0057, and RMSE of ρ on 2.13). The designed straight-line detection core processes VGA (640 × 480) videos at 0.7749 ms/frame delay on the frequency of 100 MHz.

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